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[54] ENHANCED PLANARIZATION TECHNIQUE  
FOR AN INTEGRATED CIRCUIT

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#### Related U.S. Application Data

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abandoned, which is a continuation of application No.  
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[58] Field of Search ..... 257/644, 647,  
257/634

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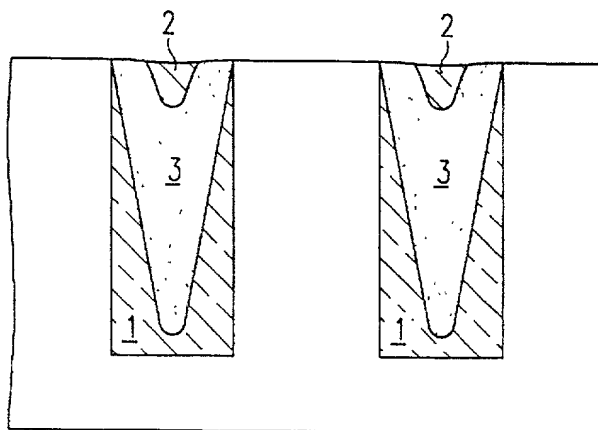
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#### [57] ABSTRACT

A method for planarizing integrated circuit topographies,  
wherein, after a first layer of spin-on glass is deposited, a  
layer of low-temperature oxide is deposited before a second  
layer of spin-on glass.

22 Claims, 4 Drawing Sheets



SOG/LTO etchback

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